
CDB47L24-M-1 Layout Guidelines

INTRODUCTION

This document describes the layout Guidelines for the CS47L24 customer board.

GENERAL BOARD CONSIDERATIONS

1. Avoid routing digital signals between power planes on an adjacent layer.

LAYOUT GUIDELINES

Note 1: Digital Signals

- Use controlled 50Ω characteristic impedance for digital signals.
- Place series termination resistors close to DUT.

Note 2: HPOUT

- HPOUTL & HPOUTR should be routed as a pair and have matched length to $\approx 5\text{mm}$.
- **Single Ended:** Route HPOUTFB between HPOUTL and HPOUTR.
- The HPOUT signal tracks should have low DC resistance. Recommended DC resistance is 1% of Min load. (0.06 Ohms for 6 ohm load)

	Min	Typ	Max	Units
DC Resistance		< 0.06		Ω

Note 3: SPKOUT

- SPKOUTP & SPKOUTN should be routed as a pair and have matched length to $\approx 5\text{mm}$.
- The speaker output should have low DC resistance tracks. (<1% of Min load)

	Min	Typ	Max	Units
DC Resistance		< 0.04		Ω

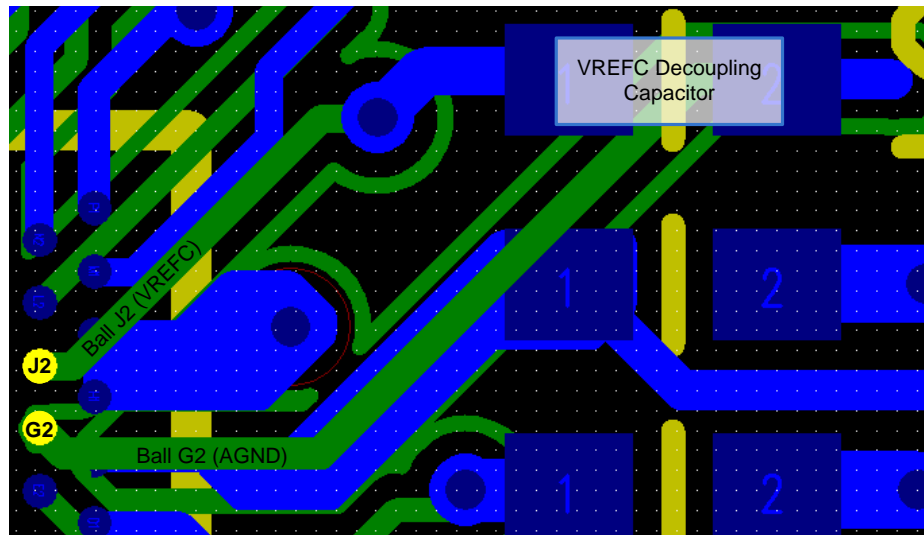
Note 4: Device Decoupling

Place de-coupling capacitors close to device.

- Note 5:** NC pins should be connected to GND for thermal relief. These pins can be left floating if required to route out signals during layout.

Note 6: VREFC GND Return

The VREFC cap current return path should be routed to AGND (Pin G2). AGND should be grounded at pin.

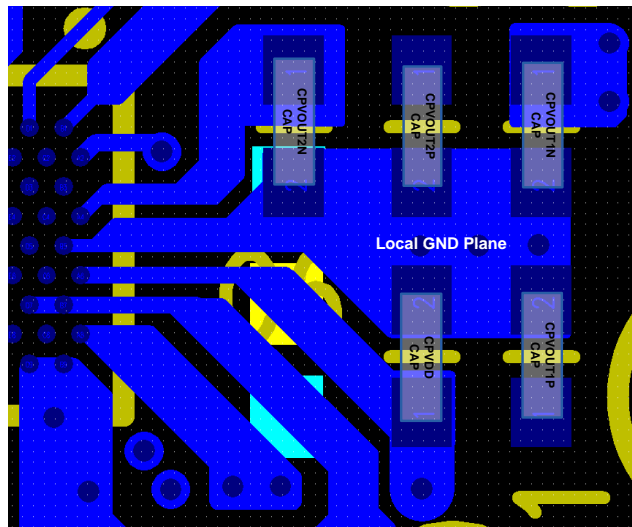
**Note 7: Charge Pump**

A local ground plane should be used for CPGND and the charge pump decoupling. The local ground plane should be connected to the common ground plane close to the CPVDD de-coupling cap.

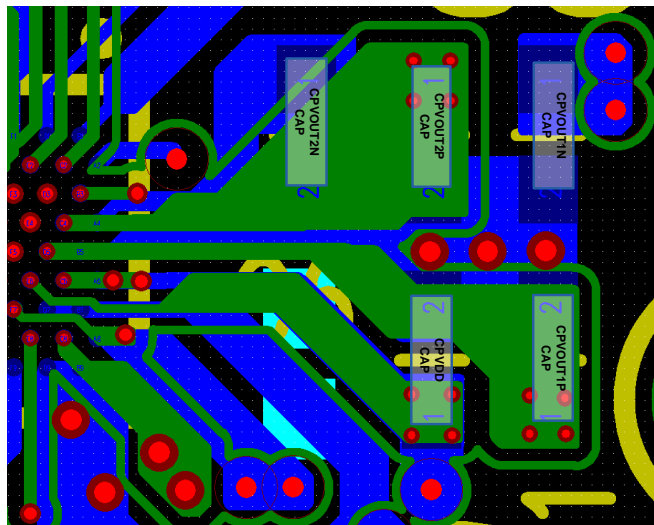
- VIAs to all GND planes should also be placed under the local ground plane. (4 - 8 VIA's)
- Order of priority in relation to charge pump components.

Priority		Notes
1	CPC2n CPGND	Headphone Charge Pump & Charge Pump Ground
2	CPVOUT2n CPVDD	Headphone Charge Pump & CPVDD
3	CPC1n	DAC Charge Pump
4	CPVOUT1n	DAC Charge Pump

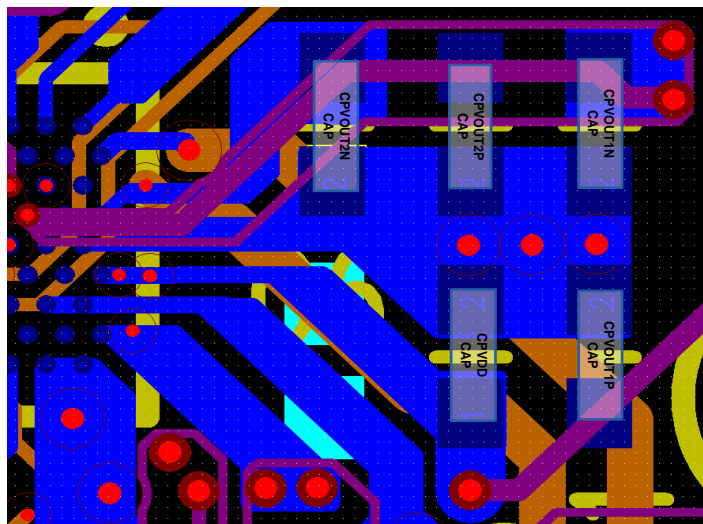
Charge Pump Layout – Top Layer



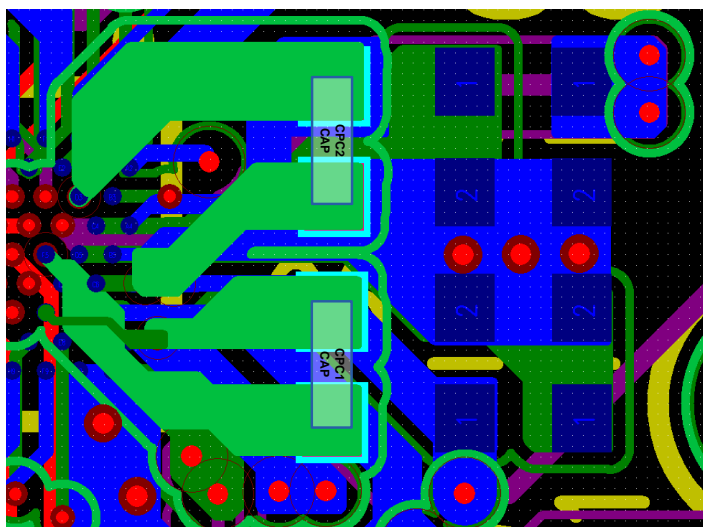
Charge Pump Layout – Layer 2



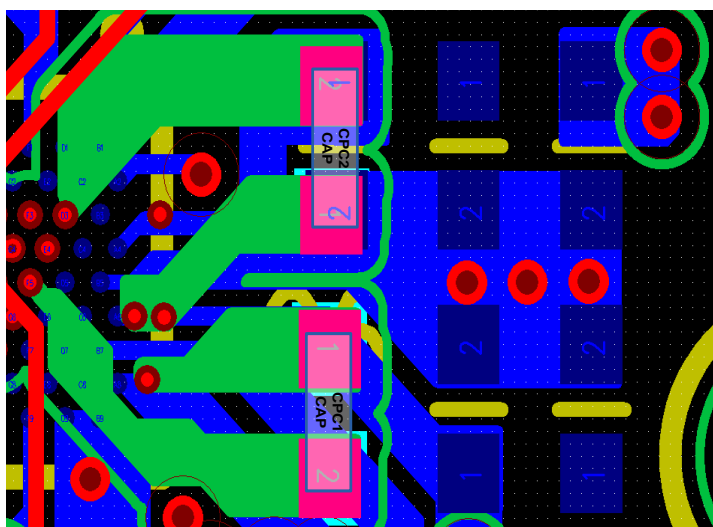
Charge Pump Layout – Layer 6



Charge Pump Layout – Layer 7



Bottom Layer



Note 8: Headphone Connections

- Star connect HPOUTFB and GND on J3:P6.
- Use a low impedance connection between J3:P6 and the ground plane.
- Use a low impedance connection between J3:P1 and the ground plane.

TECHNICAL SUPPORT

If you require more information or require technical support, please contact one of the Cirrus Logic regional offices. To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	PAGE	CHANGED BY
11/03/2016	1.0	Original document created		Craig McAdam

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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